IN THE CLAIMS

The text of all pending claims, along with their current status, is set forth below:

1-11. (Cancelled)

12. (Original) A transistor comprising:

a drain terminal comprising a doped polysilicon material disposed within a first shallow cavity formed in an isolation oxide region;

a source terminal comprising a polysilicon material disposed within a second shallow cavity formed in the isolation oxide region;

a channel formed in a silicon material and arranged between each of the first shallow cavity and the second shallow cavity, wherein the channel comprises a respective doped region coupled to each of the drain terminal and the source terminal; and

a gate disposed over the channel and comprising one or more conductive layers disposed over a gate oxide layer.

13. (Original) The transistor, as set forth in claim 12, wherein each of the plurality of cavities comprises a depth in the range of approximately 300 angstroms to 1500 angstroms.

14. (Original) The transistor, as set forth in claim 12, wherein each of the plurality of cavities comprises an aspect ratio of less than or equal to approximately 0.5 to 10.

15. (Original) The transistor, as set forth in claim 12, wherein each of the plurality of cavities comprises an aspect ratio of less than or equal to approximately 1 to 3.

16. (Original) The transistor, as set forth in claim 12, comprising:

a first conductive post coupled to the drain terminal and extending vertically therefrom; and

a second conductive post coupled to the source terminal and extending vertically therefrom;

wherein each of the first and second conductive posts are coupled to the respective drain and source terminals at a distance from the gate that is greater than 50% of the width of the respective drain and source terminals.

17. (Original) A memory device comprising:

a storage device; and

a transistor coupled to the storage device, wherein the transistor comprises:

a drain terminal comprising a doped polysilicon material disposed within a first shallow cavity formed in an isolation oxide region;

a source terminal comprising a polysilicon material disposed within a second shallow cavity formed in the isolation oxide region;

a channel formed in a silicon material and arranged between each of the first shallow cavity and the second shallow cavity, wherein the channel comprises a respective doped region coupled to each of the drain terminal and the source terminal; and

a gate disposed over the channel and comprising one or more conductive layers disposed over a gate oxide layer.

18. (Original) The memory device, as set forth in claim 17, wherein the storage device comprises a capacitor.

19. (Original) The memory device, as set forth in claim 17, wherein each of the plurality of cavities comprises a depth in the range of approximately 300 angstroms to 1500 angstroms.

20. (Original) The memory device, as set forth in claim 17, wherein each of the plurality of cavities comprises an aspect ratio of less than or equal to approximately 0.5 to 10.

21. (Original) The memory device, as set forth in claim 17, wherein each of the plurality of cavities comprises an aspect ratio of less than or equal to approximately 1 to 3.

22. (Original) A system comprising:

a processor; and

a memory device coupled to the processor and comprising:

a storage device; and

a transistor coupled to the storage device, wherein the transistor comprises:

a drain terminal comprising a doped polysilicon material disposed within a first shallow cavity formed in an isolation oxide region;

a source terminal comprising a polysilicon material disposed within a second shallow cavity formed in the isolation oxide region;

a channel formed in a silicon material and arranged between each of the first shallow cavity and the second shallow cavity, wherein the channel comprises a respective doped region coupled to each of the drain terminal and the source terminal; and

a gate disposed over the channel and comprising one or more conductive layers disposed over a gate oxide layer.

23. (Original) The system, as set forth in claim 22, wherein each of the plurality of cavities comprises a depth in the range of approximately 300 angstroms to 1500 angstroms.

24. (Original) The system, as set forth in claim 22, wherein each of the plurality of cavities comprises an aspect ratio of less than or equal to approximately 0.5 to 10.

25. (Original) The device, as set forth in claim 22, wherein each of the plurality of cavities comprises an aspect ratio of less than or equal to approximately 1 to 3.

26-32. (Cancelled)